Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A semiconductor structure comprising:

an active layer of a semiconductor material, said active layer including a strained region;

a substrate; and

an insulating layer disposed between said active layer and said substrate, said insulating layer containing a thickened region underlying said strained region, and said thickened region transferring tensile stress to said strained region.

2. (Original) The semiconductor structure of claim 1 wherein said insulating layer is a buried oxide layer and said active layer is silicon.

3. (Original) The semiconductor structure of claim 1 further comprising:

a source defined in said active layer;

a drain defined in said active layer; and

a channel defined in a portion of said active layer between said source and said drain, said channel disposed at least partially in said strained region of said active layer.

4. (Original) The semiconductor structure of claim 3 further comprising:

a gate electrode electrically isolated from said portion of said active layer defining said channel.

5. (Original) The semiconductor structure of claim 4 wherein said strained region divides said gate electrode.

6. (Original) The semiconductor structure of claim 4 wherein said gate electrode generally overlies said channel.

7. (Original) The semiconductor structure of claim 1 further comprising:

a semiconductor device fabricated using said active layer.

8. (Original) The semiconductor structure of claim 1 wherein said active layer is silicon and said thickened region of said insulating layer is formed by oxidation of said active layer.

9. (Original) The semiconductor structure of claim 9 wherein said insulating layer is silicon dioxide.

10. (Original) The semiconductor structure of claim 9 wherein said substrate is silicon and said thickened region is formed by oxidation of said substrate.

11. (Original) The semiconductor structure of claim 1 wherein said tensile stress is effective to enhance carrier mobility within said strained region.

12. (Original) The semiconductor structure of claim 1 wherein a thickness of said thickened region is increased by an increment in the range of about 5 nanometers to about 10 nanometers.

13. (Original) The semiconductor structure of claim 1 wherein said thickened region of said insulating layer has a thickness greater than that of surrounding regions of said insulating layer flanking said thickened region.

14. (Original) The semiconductor structure of claim 1 further comprising:

first and second anchors flanking said strained region, said first and second anchors effective for limiting relaxation of said strained region of said active layer.

15. (Original) The semiconductor structure of claim 16 wherein said first and second anchors comprise adjacent regions of said active layer flanking said strained region.

16-34. (Cancelled)